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1. **BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI**
2. **WORK-INTEGRATED LEARNING PROGRAMMES DIVISION**
3. **B Tech(Information Systems) in collaboration with WIPRO**
4. **Second Semester 2022-2023(July 2023)**

**COURSE HANDOUT**

**Part A: Content Design**

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| --- | --- |
| **Course Title** | DIGITAL ELECTRONICS AND MICROPROCESSOR |
| **Course No(s)** | SEWI ZC261 |
| **Credit Units** | 4 |
| **Course Author** |  |
| **Version No** | 2.0 |
| **Date** |  |

**Course Objective**

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| **No** | **Course Objective** |
| **CO1** | The course aims at understanding the fundamentals of Digital electronics (Building Blocks of digital systems, Boolean algebra etc). |
| **CO2** | Understand Digital System Design ( combinational and sequential circuits ) and understand its practical application in day to day life. |
| **CO3** | Learn the basic microprocessor Architecture, Instruction set, programming, interfacing memory and IO which will enable students to design a microprocessor based systems for different applications. |

**Text Book(s)**

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| --- | --- |
| T1 | Mano, M. Morris, Michael D. Ciletti, Digital Design, Pearson Education, 5th Edition. |
| T2 | Barry B. Brey, The Intel Microprocessors, Architecture, Programming and Interfacing, PearsonEducation, 8th Ed., 2009. |

**Reference Book(s) & other resources**

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| --- | --- |
| R1 | Douglas V Hall, Microprocessors and Interfacing, mcGraw-Hill, revised second edition.2006 |
| R2 | B. Ram , Fundamentals of Microprocessor and Microcontrollers , DhanpatRai publications. |
| R3 | Ronald J. Tocci, Digital Systems: Principles and Applications, 10th Ed, Pearson Education |
| R4 | David Money Harris and Sarah L. Harris, Digital Design and Computer Architecture (Books24X7) |
| R5 | A. Saha and N. Manna, Digital Principles and Logic Design (Books24X7) |

**Modular Content Structure**

**1. Digital Systems and Numbering systems**

1.1 Introduction to Digital systems and number systems

1.2 Binary Numbers

1.3 Number base Conversion

1.3.1 Decimal, Binary, Octal, hexadecimal Number base conversion.

1.4 Complements

1.5 Binary logic

**2. Boolean Algebra and Logic Gates**

2.1 Basic Theorems and Properties of Boolean Algebra

2.2 Boolean Functions

2.3 Canonical and Standard Forms

2.4 Digital Logic Gates

**3. Gate Level Minimization**

3.1 Introduction

3.2 The K- Map Method

3.3 SOP/POS Simplification

3.4 Don’t Care Conditions

3.5 NAND and NOR Implementations

**4. Combinational Logic**

4.1 Introduction to Combinational Circuits

4.2 Analysis and Design procedure

4.3 Binary Adder – Subtractor

4.4 Decimal Adder

4.4.1 BCD Adder

4.5 Binary Multiplier

4.6 Magnitude Comparator

4.7 Decoders

4.8 Encoders

4.9 Multiplexers

4.10 De-Multiplexers

**5. Synchronous Sequential Circuits**

5.1 Introduction to sequential circuits

5.2 Storage Elements: Latches and Flip-flops

5.2.1 SR Flip Flop

5.2.2 JK Flip Flop

5.2.3 D Flip Flop

5.2.4 T Flip Flop

5.2.5 Master –Slave Flip Flop

5.2.6 Characteristic tables and equations of flip flops

5.3 Analysis of Clocked Sequential Circuits

5.4 State Reduction

**6. Registers and Counters**

6.1 Registers

6.2 Shift Registers

6.3 Ripple Counters

6.4 Synchronous Counters

6.5 Other counters

**7. The Microprocessors and Its Architecture**

7.1 Introduction to Microprocessor

7.2 A Historical Background

7.3 The Microprocessor Based Personal Computer System

7.4 Internal Microprocessor Architecture

7.4.1 Programming Model

7.4.2 Multipurpose Registers

7.5 Real Mode Memory Addressing

7.5.1 Default Segment and Offset Registers

7.5.2 Segment and Offset Addressing Schemes

**8. 8086 Hardware Specifications**

8.1 Pin-Outs and Pin Functions

8.2 Bus Buffering and Latching

8.2.1 Demultiplexing the Buses

8.3 Bus Timing

8.3.1 Basic Bus Operation

8.3.2 Read Timing

8.3.3 Write Timing

**9. Addressing Modes**

9.1 Data Addressing Modes

9.1.1 Register Addressing

9.1.2 Immediate Addressing

9.1.3 Direct Data Addresssing

9.1.4 Register Indirect Addressing

9.1.5 Base Plus Index Addressing

9.1.6 Register Relative Addressing

9.1.7 Base Plus Index Addressing

9.2 Program Memory Addressing Modes

9.2.1 Direct Program Memory Addressing

9.2.2 Relative Program Memory Addressing

9.2.3 Indirect Program Memory Addressing

9.3 Stack Memory Addressing Modes

**10. Instruction Set and Programming Of 8086 Microprocessor**

10.1 Data Movement Instructions

10.1.1 MOV Instruction Revisited

10.1.2 PUSH/POP Instructions

10.1.3 Load-Effective Address

10.1.4 String Data Transfers

10.1.5 Miscellaneous Data Transfer Instructions

10.1.6 Introduction to Assembler

10.2 Arithmetic and Logic Instructions

* + 1. Addition, Subtraction and Comparison
    2. Multiplication and Division
    3. BCD and ASCII Arithmetic
    4. AND/OR/EX-OR Instructions
    5. TEST and BIT Instructions
    6. NOT and NEG Instructions
  1. Shift and Rotate Instructions
  2. String Comparision Instructions

10.5 Program Control Instructions

**11. Memory Interface**

11.1 Memory devices

11.2 Address decoding Techniques

11.3 Interfacing RAM and ROM devices with Microprocessor

**12. I/O Interfacing**

12.1 Introduction to I/O Interface

12.2 Programmed I/O

12.3 I/O port address Decoding

12.4 I/O Interfacing Techniques

12.4.1 I/O Mapped I/O and Memory Mapped I/O

12.4.2 Interfacing of 8 bit Input and Output Port

12.4.3 Interfacing 16 bit Input / Output device

12.4.4 Key pad Interfacing

12.4.5 LED Interafcing

12.5.5 Seven Segment Display Interfacing

12.5.6 A/D Converter Interfacing

12.5.7 Stepper Motor Control Interface and System Design Exmple

**13. Interrupts**

13.1 Introduction To interrups

13.2 8086 Interrupt Types

13.2 .1 Divide by Zero(Type 0)

13.2.2 Single step Interrupt(Type 1)

13.2.3 Non MaskableInterrupt(Type 2)

13.2.4 Break point Interrupt(Type 3)

13.2.5 Overflow Interrupt(Type 4)

13.2.6 Software Interrupts

13.2.7 MaskableInterrupt(INTR)

13.3 Interrupt priorities

**Learning Outcomes:**

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| --- | --- |
| No | Learning Outcomes |
| LO1 | An ability to **infer** number systems, Boolean algebra and minimize logic function using K-map method. |
| LO2 | Ability to **analyze and design** combinational logic networks in a hierarchical, modular approach, using standard and custom logic blocks. |
| LO3 | Ability to **analyze and design** basic synchronous sequential machines using various memory elements. |
| LO4 | Ability to **apply** digital system design principles and descriptive techniques. |
| LO5 | Ability to understand basic elements, functions and architecture of a microprocessor and **analyze, specify, design**, write and test assembly language programs of moderate complexity |
| LO6 | Ability to **develop** software using assembly language to control an application interface microprocessor using various peripheral devices. |

**Part B: Contact Session Plan**

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| **Academic Term** |  |
| **Course Title** | DIGITAL ELECTRONICS AND MICROPROCESSOR |
| **Course No** |  |
| **Lead Instructor** |  |

**Course Contents**

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| --- | --- | --- | --- |
| **Contact Hour** | **List of Topic Title**  **(from content structure in Part A)** | **Topic #**  **(from content structure in Part A)** | **Text/Ref Book/external resource** |
| 1 | **Digital Systems and Numbering Systems:**Digitalsystems,Binary Numbers, Number base Conversion, Decimal, Binary, Octal, hexadecimal Number base conversion.Complements,Binary logic, Signed Binary, Binary codes, . | 1.1- 1.5 | T1- 1.1, 1.2. 1.3, 1.4, 1.5, 1.6, 1.7, 1.8 |
| 2 | **Boolean Algebra and Logic Gates:** Basic Theorems and Properties of Boolean Algebra, Boolean Functions | 2.1, 2.2 | T1- 2.1, 2.2, 2.3, 2.4, 2.5 |
| 3 | **Boolean Algebra and Logic Gates**  Canonical and Standard Forms,Digital Logic Gates | 2.3, 2.4 | T1- 2.6, 2.7, 2.8 |
| 4 | **Gate Level Minimization:** Introduction,The Map Method-Two, Three and Four Variable Map, Product of Sums Simplification,Don’t Care Conditions, NAND and NOR Implementations. | 3.1, 3.2, 3.3, 3.4,3.5 | T1- 3.1, 3.2, 3.3, 3.4, 3.5, 3.6, 3.7 |
| 5 |
| 6 | **Combinational Logic :**  Introduction to Combinational Circuits, Analysis and Design procedure, Binary Adder – Subtractor, | 4.1, 4.2, 4.3 | T1- 4.1, 4.2, 4.3, 4.4, 4.5 |
| 7 |
| 8 | **Combinational Logic**: Decimal Adder, Binary Multiplier, Magnitude Comparator, Decoders | 4.4, 4.5, 4.6, 4.7 | T1-4.6, 4.7, 4.8, 4.9 |
| 9 | **Combinational Logic:** Encoders, Multiplexers, De-Multiplexers | 4.8, 4.9, 4.10 | T1- 4.10, 4.11 |
| 10 |
| 11 | **Synchronous Sequential Circuits:** Introduction, Storage Elements: Latches and Flipflops | 5.1, 5.2 | T1- 5.1, 5.2, 5.3, 5.4, R5 |
| 12 | **Synchronous Sequential Circuits:** Analysis of Clocked Sequential Circuits, State Reduction | 5.3, 5.4 | T1- 5.5, 5.7, 5.8 |
| 13 | **Registers and Counters:** Registers, Shift Registers | 6.1, 6.2 | T1- 6.1, 6.2 |
| 14 | **Registers and Counters:** Ripple Counter, Synchronous Counters, Other Counters | 6.3, 6.4, 6.5 | T1- 6.3, 6.4, 6.5 |
| 15 |
| 16 | **The Microprocessors and Its Architecture:** Introduction to Microprocessor, A Historical Background, The microprocessor Based Personal Computer System. | 7.1, 7.2, 7.3 | T2- 1.1, 1.2 |
| 17 | **The Microprocessors and Its Architecture:I**nternal Microprocessor Architecture, Programming Model, Multipurpose Registers, Real Mode Memory Addressing, Default Segment and Offset Registers, Segment and Offset Addressing Schemes | 7.4, 7.5 | T2- 2.1, 2.1, 2.3 |
| 18 | **8086 Hardware Specifications:**  Pin-Outs and Pin Functions, Bus Buffering and Latching, Demultiplexing the Buses, Bus Timing, Basic Bus Operation, Read Timing, Write Timing | 8.1, 8.2, 8.3 | T2- Ch9.1, 9.2, 9.3, 9.4, 9.5, 9.6 |
| 19 |
| 20 | **Addressing Modes:D**ataAddressing modes : Register, Immediate, Direct, Register Indirect Addressing, Base Plus Index, Register Relative, Base relative plus index Addressing | 9.1 | T2- 3.1 |
| 21 | **Addressing Modes:**  Program Memory Addressing Modes, Stack Memory Addressing Modes. Examples for Program and Stack Memory Addressing | 9.2, 9.3 | T2- 3.2, 3.3 |
| 22 |
| 23 | **Instruction Set and Programming Of 8086 Microprocessor :** Data Movement Instructions: MOV, PUSH/POP, Load effective Address, String data Transfers,Miscellaneous Data Transfer Instructions, Segment Override Prefix, Introduction to Assembler | 10.1 | T2- 4.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7 |
| 24 | **Instruction Set and Programming Of 8086 Microprocessor** :Arithmetic and Logic Instructions, Shift and Rotate Instructions, Program Control Instructions | 10.2, 10.3, 10.4, 10.5 | T2- 5.1, 5.2, 5.3, 5.4, 5.5, 5.6, 6.1,6.2, 6.3, 6.5 |
| 25 |
| 26 | **Memory Interface:** Memory devices, Address decoding Techniques, Interfacing RAM and ROM devices with Microprocessor. | 11.1, 11.2, 11.3 | T2- Ch 10 |
| 27 |
| 28 | **I/O Interfacing:** Introduction to I/O Interface, Programmed I/O, I/O port address Decoding,I/O Interfacing Techniques, Interfacing of 8 bit Input /Output device, Interfacing 16 bit Input / Output device. | 12.1, 12.2, 12.3, 12.4 | T2- 11.1, 11.2, 11.3, 11.4, 11.6, |
| 29 |
| 30 | **Interrupts:** Introduction , 8086 Interrupt Types(Hardware/Software Interrupts), Interrupt priorities | 13.1, 13.2, 13.3 | T2- 12.1, 12.2, 12.5 |
| 31 | Review Session |  |  |
| 32 | Review Session |  |  |

**Detailed Plan for Lab work/Design work:**

* Infrastructure Needed:
* Simulation software Multisim for Digital Electronics
* EMU8086 for Microprocessor
* Lab Sessions required: 5-6 sessions.

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| **Lab No** | **Lab Objective** | **Lab Sheet Access URL** | **Content Reference** |
| 1 | Realization of all Basic gates using Universal Gates (Both NAND and NOR) using multisim. |  | Lab Sheets |
| 2 | Simplification , Realization of Boolean Expressions by using Logic gates/Universal Gates using multisim. |  | Lab Sheets |
| 3 | Design of combinational circuit using multisim(Adder/Subtractor/comparator/MUX/DEMUX) |  | Lab Sheets |
| 4 | Design of MOD N counter (synchronos/Asynchronous) using IC 7476 using multisim. |  | Lab Sheets |
| 5 | A. Byte and word data transfer in different  addressing modes .  B.To transfer a block of data with out overlap  C. Block Exchange |  | Lab Sheets |
| 6 | A. 16 bit Addition/ Subtraction/ Multiplication  B. LCM of Two Numbers |  | Lab Sheets |
| 7 | Program to find Largest /Smallest in the Array. |  | Lab Sheets |
| 8 | Sorting Array in Ascending/Descending Order |  | Lab Sheets |
| 9 | Program to transfer a String from one location to another. |  | Lab Sheets |